High Density SiC MOSFET Converters for Medium Voltage

- MVDC distribution in highly populated URBAN areas
- Electric ship DC power system and propulsion motor drive

Land or space is limited and expensive
Requires high-density, high-efficiency converters

Most suitable converter/control: Switching-Cycle Control (SCC) of MMC

- Capacitor ripple: 100 % Conv., 7 % SCC, 14x reduction
- Inductance: 100 % Conv., 26 % SCC, 3.8x decrease
- Losses: 100 % Conv., 90 % SCC, 90 % reduction

High-density
High-efficiency

High density
High speed
High efficiency

Kernel part: SiC MOSFET

Power Cell

Vdc
n

April 22th, 2021
Center for Power Electronics Systems
6 kV Power-Cell for SCC MMC Converter

Wireless Auxiliary supply

GD Power Supply

Gate Driver (GD)

Inductor

Local Controller

Digital Sensors

Aux. circuits:

Pre-charge

Mini-UPS

XHV6 (3xXHV9) SiC MOSFET

PCB Planar Busbar

*CPES 2020

April 22th, 2021
Center for Power Electronics Systems
Extraordinary characteristics of SiC MOSFETs: high breakdown voltage, fast switching speed, low losses, and higher operating temperature

High voltage (≥10 kV) SiC enables simplification of power stage topologies, preserving the overall harmonic performance, meanwhile having high efficiency and improving power density

Applications: electric grid interface, electric ships, renewable energy sources
Background: Objectives and Challenges

- Modular multilevel converter (MMC) exhibits salient features such as **high modularity, voltage scalability, transformerless operation, and low filter requirements**.

### Power-cell Objectives

- ICBT and SCC control modes
- Efficiency > 99% at full load (97% at light load)
- Power density > 10 kW/l
- >100 V/ns immunity
- High Degree of Intelligence
- PD free operation
- Complete modularity

### Challenges

- High-voltage Isolation
- Noise Immunity – High EMI (dv/dt)
- Thermal Management
Power Cell Assessment Methodology

Power-Cell Design

Device Static Characterization
If not known through datasheet: IV curves ($R_{ds,on}$, $V_{gs,th}$, $V_{breakdown}$), transconductance $g_m$, capacitances $C_{iss}$, $C_{oss}$, $C_{rss}$

Power-Cell Insulation Testing
- Frame (earth gnd) to heatsink
- Frame (earth gnd) to dc-side
- Frame (earth gnd) to ac side

Dynamic Characterization
- Device dynamic losses
- On/off times, etc

Power-Cell Safe Operation Area
Identify the SOA based on combination of:
- Power-cell device characterization
- Thermal model

Power-Cell Safe Operation Area Assessment
- Basic functionality dc-dc, dc-ac testing
- Thermal characterization and model verification
- EMI characterization
- Efficiency characterization

System-level Test Type
Regenerative circulating power
- Reactive power
- Pumpback
Non-regenerative active power
- Direct load

Final Design

No
Passed
Yes

Passed

September 1st, 2020

Center for Power Electronics Systems
Safe Operation Area

Most suitable for lab conditions due to:
- Load is mirror converter
- High voltage, low current source
- Easy and practical for loss measurement

Defined for dc-dc case, 50% duty cycle, 150°C
- Complete static characterization
- Complete dynamic characterization
- Accurate thermal model
Operation Verification: dc-dc

\[ v_{\text{ind}} = v_{\text{ds2}} - v_{\text{ds4}} \]

\[ f_{\text{sw}} = 10 \text{ kHz} \]
Thermal Management

6 kV, 84 A, 10 kHz, dc-dc mode

\[ T_{j,est,S1} = 109^\circ C \]

Multi-point Thermal Model Verification

\[ \Delta T = 4 - 8^\circ C \approx 10\% \]
EMI Characterization

Cross-talk Evaluation

Gate driver Common-mode Transient Immunity

\[ i_{rss} = C_{rss} \cdot \frac{dv_{ds}}{dt} \]

\[ \Delta V_{gs} = R_{g,\text{tot}} \cdot i_{rss} \cdot (1 - e^{-\frac{t_{sp}}{\tau}}) \]

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September 1st, 2020
Discrepancy between estimated and measured: 0.35%

Peak Power-Cell Efficiency $\eta = 99.6$ (5 kHz)
Peak Power-Cell Efficiency $\eta = 99.3$ (10 kHz)
Performance changes requires often adjustments.
Reliability concerns over time: reduces usable lifetime.
Proposed Solution: Digital Self-Calibration

- Viable substitute that eliminates mechanical related reliability issues and in-person retuning of the system is digital (electronic) potentiometer.

- Rogowski coil self-calibration is executed either at the start-up of the gate-driver or can be requested from user.
Modular, scalable medium-voltage converter

Background, Motivation and Design Specs

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Design Specifications

- **Inductance**: 2 μH
- **Current (50% nominal)**:
  - avg: 32 A, rms: 126 A, max: 484 A
- **Voltage**: DM: 6 kV, CM: ±3 kV
- **dv/dt**: up to 100 V/ns
- **Switching frequency**: 40 kHz

Medium voltage

Bulk insulation

High power density

Narrow space for passive components

Larger size

Smaller size
Design Structure Selection and Optimization

- **Selected structure:**
  Single-turn magnetic-core inductor with shielded solid insulation

- **Shield loss – conductivity and thickness selection**
  - **Conductive**
    - Equipotential surface
    - Insulation safety
    - Higher loss
  - **Resistive**
    - Lower loss
    - Voltage on shield is non-uniform
    - Potential HV insulation issues

- **Shield termination design**
  - **Geometric solution**
    - Least compact
  - **Resistive solution**
    - Easily manufacturable
    - Dependent on frequency
  - **Refractive solution**
    - Most compact
    - Significant difficulties in manufacturing
  - **Capacitive solution**
    - Most compact
    - Significant difficulties in manufacturing

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Sponsored by ONR / ARPA-E
A Compact Termination Structure Design

- **Refractive solution: high–ε stress control layer**

  - Shield
  - Conductor
  - Insulator
  - Stress control layer

  \[ E (kV/mm) \times x_2 (mm) \]

  \[ E (kV/mm) \times x_1 (mm) \]

  - Case c is a good tradeoff between \( E_{\text{max}} \) on \( x_1 \) and \( x_2 \)

- **Why do we need double-layer termination?**

  - Shield
  - Additional layer (high \( \varepsilon_r \))
  - Additional layer (low \( \varepsilon_r \))

- **How to determine the thickness and permittivity?**

  - \( E_{\text{max}} \) on \( x_1 \)
  - \( E_{\text{max}} \) on \( x_2 \)
Shield Grounding Current Reduction

C_{dc} \quad L_{PEBB} \quad C_{dc}

R_{end} \quad C_{end,eqt} \quad 0.5L \quad 0.5R_{bar} \quad 0.5L \quad 0.5R_{bar} \quad R_{end}

C_{end,eqt} \quad 0.5M \quad C_{P} \quad 0.5M \quad 0.5M \quad C_{end,eqt}

Copper-bar
Insulator
Termination

Shielding layer
Cores

Insulator
Termination
Shielding layer
Cores

Peak current [A]
RMS current (A)
Grounding loss (W)
Peak voltage on shield (V)

Grounding resistance [\Omega]
Grounding resistance [\Omega]
Grounding resistance [\Omega]
Grounding resistance [\Omega]

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Lab Fabrication Process

- **Insulation fabrication method 1:**
  - Copper bar preparation ➔ Mica tape wrapping ➔ Release agent applying ➔ Hot press curing ➔ Oven curing ➔ Sanding and shaping

- **Insulation fabrication method 2:**
  - Mold 3D printing ➔ Acetone vapor polishing ➔ Applying release agent ➔ Casting material preparation ➔ Degassing and curing ➔ Demolding

- Shielding ➔ Adding termination ➔ PEBB integration

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Lab Fabrication Process

- Copper bar preparation
- Insulation fabrication
- Shielding
- Adding termination

PEBB integration

(Fabrication examples)
Measurements and Test Validation

<table>
<thead>
<tr>
<th></th>
<th>Inductance</th>
<th>Parasitic capacitance</th>
<th>PDIV (peak voltage)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fabrication method 1</td>
<td>2.508 μH</td>
<td>263.59 pF</td>
<td>5.16 kV</td>
</tr>
<tr>
<td>Fabrication method 2</td>
<td>2.573 μH</td>
<td>177.31 pF</td>
<td>7.34 kV</td>
</tr>
</tbody>
</table>

32.7% reduction!

42.3% increasement!
Outline

- Research Background
- Switching-cycle Control (SCC) Principle
- Control Partition and Distribution
- Synchronization and Temporal Cooperation
- Experimental Verifications
**Research Background**

- **Technical Challenges for Conventional Modular Multilevel Converters (MMC)**
  - Capacitor voltage ripple inversely proportional to line-frequency → Large passive components
  - Voltage ripples $\propto \frac{1}{f_1}$
  - Higher than 10 times reduction on passive components (cell capacitors and arm inductors)
  - ZVS achieved without additional components

- **Switching-cycle control (SCC)**
  - Higher than 10 times reduction on passive components (cell capacitors and arm inductors)
  - ZVS achieved without additional components

![Diagram illustrating MMC with 2nd order harmonic injection and MMC with 2nd + HF harmonic injection with SCC control]
**Switching-cycle Control (SCC) Principle**

- **Capacitor voltage switching-cycle balancing**
  
  *Segmented arm currents → Capacitor charge & discharge balancing*

\[
i_{\text{CIR}} = \frac{(i_U + i_L)}{2}
\]
## Control Partition and Distribution

### Control partition

**Five-layer control partition**

<table>
<thead>
<tr>
<th>Control Type</th>
<th>Layer</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>System control</td>
<td>mS</td>
<td>User interface</td>
</tr>
<tr>
<td>Application control</td>
<td>µS</td>
<td>Operating mode state machine</td>
</tr>
<tr>
<td>Converter control - a</td>
<td>µS</td>
<td>Output current regulation, Capacitor voltage sorting</td>
</tr>
<tr>
<td>Converter control - b</td>
<td>µS</td>
<td>Arm current reference, Duty cycle calc, ACM or PCM selection</td>
</tr>
<tr>
<td>Switching control</td>
<td>ns</td>
<td>ACM or PCM modulation</td>
</tr>
<tr>
<td>Hardware control</td>
<td>ns</td>
<td>Interlock and deadline, Fault detection and protection, Capacitor voltage sensing, Device current sensing</td>
</tr>
</tbody>
</table>

### Distributed control system

**Main, cell and gate-driver controller**

- 5 Gbps Ethernet connection
- 50 Mbps Ethernet connection
- MMC Cell +
- Gate driver controller
- Cell controller
- Optical fibres

- Main controller
- Optical fibres
- Gate driver controller
- Cell controller
- 50 Mbps Ethernet connection
- 5 Gbps Ethernet connection
**Synchronization and Temporal Cooperation**

- Tasks are scheduled among tightly-synchronized distributed controllers

- **Main Controller x 1**
  - Current sensor
  - FPGA
  - ARM core

- **Cell Controller x 2n**
  - Voltage sensor
  - FPGA
  - ARM core

- **Gate Driver Controller x 4n**
  - FPGA

- **Functions**
  - Sampling
  - Communication
  - Cap voltage sorting
  - Phase current regulation
  - State machine
  - User interface
  - SCC Arm current boundary calculation
  - Average-current mode & Peak-current mode modulation
  - Fault detection

- ~ns synchronization
Experimental Verifications

- 10 kV SiC MOSFET-based half-bridge power cell
  
  ![Half-bridge power cell diagram]

- Control hardware synchronization verifications
  
  ![Control hardware synchronization diagram]

- MMC cell PCM modulation verification at 6 kV and 80 A
  
  ![MMC cell PCM modulation verification diagram]